AMENDMENTS TO THE CLAIMS

1-8. (Canceled)

9. (Previously Amended) A method, comprising:

forming a first dielectric layer on a semiconductor substrate;

forming a floating gate above the first dielectric layer, the floating gate comprised of a first polysilicon layer doped with a first type of dopant material and a second polysilicon layer doped with a second type of dopant material that is opposite the first type of dopant material in the first polysilicon layer, wherein forming the floating gate comprises depositing the first polysilicon layer above the dielectric layer and depositing the second polysilicon layer above the first polysilicon layer;

forming a second dielectric layer above the floating gate;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate.

10. (Original) The method of claim 9, wherein forming the first polysilicon layer above the dielectric layer and the second polysilicon layer above the first polysilicon layer further comprises performing a first ion implantation process at a first energy to introduce dopant atoms of the first type of dopant material into the first polysilicon layer and performing a second ion implantation process at a second energy to introduce dopant atoms of the second type of dopant material into the second polysilicon layer with a second dopant, wherein the first energy is larger than the second energy.

11. (Original) The method of claim 10, wherein performing the ion implantation process at the first energy comprises performing the ion implantation process at the first energy such that the ion implant range is at about a mid-point of the first polysilicon layer and a first dopant dose of approximately 10^{10} - 10^{15} atoms/cm^2.

12. (Original) The method of claim 11, wherein performing the ion implantation process at the second energy comprises performing the ion implantation process at the second energy such that the ion implant range is at about a mid-point of the second polysilicon layer and a second dopant dose of approximately 10^{13} -10^{16} atoms/cm^2.

13-24. (Canceled)

25. (Previously Amended) A method, comprising:

forming a first dielectric layer on a semiconductor substrate;

depositing a first polysilicon layer above the first dielectric layer;

forming a barrier layer above the first polysilicon layer;

depositing a second polysilicon layer above the barrier layer;

performing a first ion implantation process to introduce a first type of dopant material into the first polysilicon layer using a first dopant dose of approximately 10^{10} - 10^{15} ions/cm^2 at a first energy such that an ion implant range is at about a mid-point of the first polysilicon layer;

performing a second ion implantation process to introduce a second type of dopant material into the second polysilicon layer using a second dopant dose of approximately 10^{13} - 10^{16} ions/cm^2 at a second energy, wherein the first energy is larger than the second energy;

forming a second dielectric layer above the second polysilicon layer;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate.

26. (Canceled)

27. (Previously Amended) A method, comprising:

forming a first dielectric layer on a semiconductor substrate;

depositing a first polysilicon layer above the first dielectric layer;

forming a barrier layer above the first polysilicon layer;

depositing a second polysilicon layer above the barrier layer;

performing a first ion implantation process to introduce a first type of dopant material into the first polysilicon layer using a first dopant dose of approximately 10^{10} - 10^{15} ions/cm^2 at a first energy;

performing a second ion implantation process to introduce a second type of dopant material into the second polysilicon layer using a second dopant dose of approximately 10^{13} - 10^{16} ions/cm^2 at a second energy such that an ion implant range is at about a mid-point of the second polysilicon layer, wherein the first energy is larger than the second energy;

forming a second dielectric layer above the second polysilicon layer;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate.

28-34. (Canceled)